Dineshkumar Bhaskaran

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Summary

- Expert in high-performance parallel computing, with a strong focus on algorithm parallelization, optimization, and benchmarking for AI/ML workloads, image processing pipelines, and distributed storage systems.
- Extensive experience in Linux kernel and systems programming, covering storage virtualization, device drivers, and board bring-ups for ARM-based architectures.

Experience

Arista Networks, Software Engineer — Vancouver, Nov 2023 - Apr 2025

- Refactored the Layer 3 Unicast routing abstraction layer, removing approximately 7K lines of redundant code between protocol and hardware interface layers.
- Unified portions of IPv4 and IPv6 handling logic using C++ templates, resulting in a cleaner codebase and 4% improvement in module build times.

AMD India, Senior Member Technical Staff — Bengaluru, Aug 2019 - Oct 2013

- **Rapids – Accelerated Data Science for ROCm:** Owned and maintained RAPIDS CUDF sub-projects (i.e. rapids-cmake, RMM, NVComp) to support PyData libraries on AMD GPUs under the ROCm stack.
- **MLPerf Inferencing:** Implemented Python reference code for models Resnet50, Yolov4 and Bert on AMD Instinct GPUs for multiple backends like pytorch, tensorflow, Tensor virtual machine (TVM) and MIGraphX. Developed a C++ inference server on TVM for ResNet50, improving performance by 51.5%.
- **ROCm Clang Compiler**
  - ROCm Clang compiler : Maintainer from Aug 2019 to Sept. 2021.
  - Implemented multithreading and in-memory compilation in AMD's Lightning compiler (based on LLVM), improving compile time by 29% on Windows and 1.07x on Linux.

Aricent (later Capgemini Engineering), Principal Engineer — Bengaluru, Oct 2017 - Jul 2019

- Developed GPU-accelerated erasure coding algorithms for CEPH. Presented results at SNIA SDC 2018 (India and Santa Clara) under the title Accelerated Erasure Coding: The New Frontiers of Software-Defined Storage – 2018.
- Implemented FFT offload in the OpenAirInterface 4G stack as part of an SDR solution, leveraging NVIDIA GPUs and Xilinx FPGAs to improve performance.

Canon Inc, Principal Engineer — Tokyo, Bengaluru, Mar 2010 - Oct 2017

- Led a team to create an efficient medical image processing library for Canon medical apparatuses. Parallelized and optimized Image registration components like Pre-processing algorithms, Optimizers (Powell, LM, GD, SGD), Metrics (MI, NMI, RIU, SSD), transformation algorithms, and Resampler.
- Managed a team that maintained and enhanced Linux based OS for Canon embedded products. Involved in porting Linux kernel and essential system applications to various ARM based SoCs.

Early Experience (Brocade communication and Tata Elxsi), Software Engineer — Bengaluru, Sep 2003 - Mar 2010

- Worked on Brocade Storage Application Services. SAS services include storage virtualization, online data migration, CDR, and CDP. Owned virtualized initiator module in SAS solution.
- Worked on Target Mode driver for LSI Logic FC HBAs based on LSI-Logic Fusion message passing technology to act as a virtualized storage box.

Education

Deep Learning Theory and Practice IISc Bengaluru
M.S Software systems 2006-2009, BITS Pilani
Bachelor of Technology, Computer Engineering 1999-2003, University of Calicut.

Technical Writing & Talks

- Blog and Assorted articles
- Accelerated Erasure Coding
- Why erasure coding is the future of data resiliency
- Writing a Network device driver

Technologies

Languages: C, HIP, OpenCL, familiar with CUDA, C++, Python, PTX, HLSL, ARM, X86 assembly.

Protocols stacks: FC, Familiar with SCSI, USB, OpenAirInterface 4G stack in Linux Kernel.

Tools and ASICs: ROCm and GNU Toolchain, Xilinx ZC-702/706, TI AM437x, AMD Instinct GPUs gfx90x series.